CLEAN SET OF CLAIMS

What is claimed is:

25. A system, comprising:
a memory array; and
a memory array controller comprising
a negative charge pump; and
a block controller coupled to the negative charge pump, comprising:
a negative level shifter to switch an output between a read-mode voltage and an erase-mode voltage dependent upon a selection signal input;
a positive voltage switch coupled to the negative level shifter;
a bit line driver coupled to the positive voltage switch and coupled to said memory array; and
a word line driver coupled to said positive voltage switch, coupled to the negative level shifter, and coupled to said memory array.

26. The system of claim 25, wherein the negative level shifter comprises an output stage comprising an n-channel transistor.

27. The system of claim 25, wherein the negative level shifter comprises an active pull-up circuit coupled to a current source pull-down circuit.

28. The system of claim 25, wherein the erase-mode voltage comprises a high magnitude negative voltage.

29. The system of claim 25, wherein the read-mode voltage comprises a low voltage current from the negative charge pump via a low resistance n-channel transistor.

30. The system of claim 25, wherein said memory array comprises a block coupled to the block controller and having a bit line, a word line, and a source line.

31. The system of claim 25, wherein said memory array controller comprises the block controller to apply a signal to a first block within said memory array to erase the first block.

32. The system of claim 25, wherein said memory array controller comprises a second block controller to apply a signal to a second block within said memory array to read a memory cell of the second block substantially simultaneously with erasure of a first block within said memory array.

33. The system of claim 25, wherein the negative charge pump comprises an output circuit to output the erase-mode voltage.

34. The system of claim 25, wherein the negative level shifter comprises an output stage circuit coupled to said memory array to apply the erase-mode voltage to a source line of said memory array.

35. The system of claim 34, wherein the output stage circuit comprises a transistor to couple the output of the negative charge pump to the source line.

36. The system of claim 25, wherein the negative level shifter comprises a first circuit to pull up an output of the negative charge pump to apply a read-mode voltage to a first memory cell of said memory array.

37. The system of claim 36, further comprising a second negative level shifter coupled to the negative charge pump to couple the output of the negative charge pump to a second memory cell of said memory array substantially simultaneously with the application of the read-mode voltage to the first memory cell of said memory array.

38. The system of claim 36, wherein the first circuit comprises circuitry to substantially prevent current burn within the negative level shifter.

39. The system of claim 36, wherein the first circuit comprises an output stage circuit to apply a low resistance current to the first memory cell.

40. A method, comprising:

receiving a signal to erase a first block within a memory array;

lowering an output of a negative charge pump to a negative voltage;

applying the output of the negative charge pump to a source line of the first block; and

pulling up the output of the negative charge pump to apply a read-mode voltage to a memory cell of a second block within the memory array substantially simultaneously with said applying the output.

41. The method of claim 40, further comprising applying a signal to a word line and a bit line to erase the first block.

42. The method of claim 40, further comprising applying a signal to a word line and a bit line of the second block to read the memory cell substantially simultaneously with erasing the first block.

43. The method of claim 40, wherein said receiving a signal to erase a first block within a memory array comprises:

receiving an instruction to erase the first block; and

receiving an instruction to read the memory cell prior to erasure of the first block.

44. The method of claim 40, wherein said lowering an output of a negative charge pump to a negative voltage comprises lowering the output of the negative charge pump to a high magnitude, negative voltage.

45. The method of claim 40, wherein said applying the output of the negative charge pump to a source line of the first block comprises coupling the output of the negative charge pump to the source line.

46. The method of claim 40, wherein said pulling up the output comprises turning off transistors to substantially prevent current burn within a negative level shifter coupled to the second block of memory.

47. The method of claim 40, wherein said pulling up the output comprises applying a low resistance current to the memory cell.

48. An apparatus, comprising:

a negative charge pump; and

a block controller coupled to the negative charge pump, comprising:

a negative level shifter to switch an output between a read-mode voltage and an erase-mode voltage dependent upon a selection signal input; and

a positive voltage switch coupled to the negative level shifter.

49. The apparatus of claim 48, wherein the negative level shifter comprises an output stage circuit to couple to said negative charge pump to output the erase-mode voltage.

50. The apparatus of claim 48, wherein the negative level shifter comprises a first circuit to pull up an output of said negative charge pump to output a read-mode voltage.

51. The apparatus of claim 50, further comprising a second negative level shifter to couple to said negative charge pump to output an erase-mode voltage substantially simultaneously with an output of the read-mode voltage by the negative level shifter.